HEALICs

Self-HEALing RF/Mixed-Signal Integrated Circuits

Proposer's Day Workshop

June 19, 2008

PM: Sanjay Raman

This workshop is UNCLASSIFIED

Acknowledgments

- Ms. Jessica Randall
- Mr. Saverio Fazzari
- Mr. Christopher Maxey
- Dr. Phillip Chang
- Mr. John McManus/Ms. Ryann Glaccum

- Dr. Greg Kovacs, Director, DARPA/MTO
- Mr. Michael Blackstone, DARPA/CMO

- And all of you for joining us!

HEALICs Proposer's Day Agenda

Circuit, Heal Thyself!

1:00-1:15	Introductions and Agenda	Sanjay Raman, DARPA/MTO
1:15-1:45	MTO Overview and Vision	Greg Kovacs, Director, DARPA/MTO
1:45-2:15	Overview of the HEALICs BAA	Sanjay Raman, DARPA/MTO
2:15-3:00	Resiliency Efforts in the Focus Center Research Program (FCRP)	Subhasish Mitra, Stanford Univ.
3:00-3:30	Contracting for the HEALICs BAA	Michael Blackstone, DARPA/CMO
3:30-3:45	Break	
3:45-4:15	Teaming Website and TFIMS demonstration	Jessica Randall, Ryann Glaccum, Booz Allen Hamilton
4:15-5:00	Government Response to Questions	Sanjay Raman, DARPA/MTO Michael Blackstone, DARPA/CMO
5:00-6:00	Mixer and informal networking	

DARPA Organization

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Director, Tony Tether
Deputy Director, Bob Leheny

Tactical Technology
Steve Welby
Steve Walker, Dave Neyland

- Air/Space/Land/Sea Platforms
- Unmanned Systems
- Space Operations
- Laser Systems
- Precision Strike

Strategic Technology
Barbara McQuiston
Larry Stotts, Brian Pierce

- Space Sensors/Structures
- Strategic & Tactical Networks
- Information Assurance
- Underground Facility Detection & Characterization
- Chem/Bio Defense
- Maritime Operations

Defense Sciences
Brett Giroir
Leo Christodoulou

- Physical Sciences
- Materials
- Biology
- Mathematics
- Human Effectiveness
- Bio Warfare Defense

Information Processing Techniques
Charles Morefield
Charlie Holland, Mark Davis

- Cognitive Systems
- Command & Control Systems
- Computer Language Translation
- High Productivity Computing
- Sensors & Processing

Microsystems Technology
Greg Kovacs
Dean Collins

- Electronics
- Photonics
- MEMS
- Algorithms
- Integrated Microsystems

Microsystems Enabling Future System Capabilities

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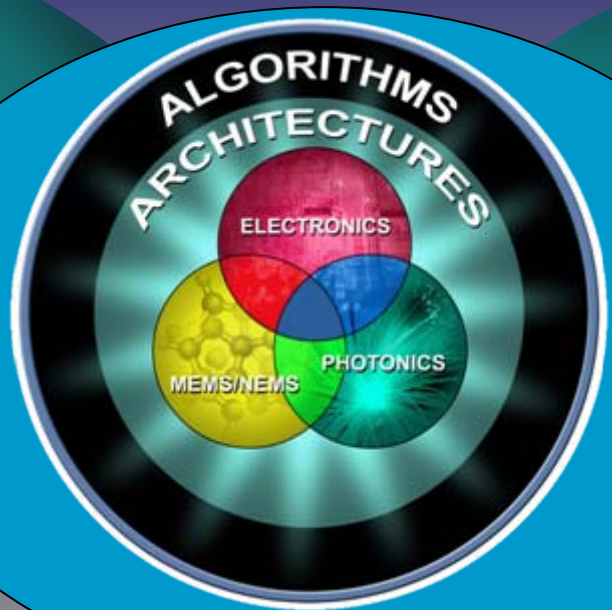
Sense:
EO/IR/Visible/UV
RF/mm-wave/THz
Chemical
Biological
Trust/Protect

Process:
Digital
Analog
Memory
Quantum
Biological
Trust/Protect



Microsystems

Communicate:
Optical
Analog/digital
Wireless RF/mm-wave

Energize:
Convert
Generate
Directed

Actuate:
Mechanical
Electrical
Optical
Chemical

DARPA / MTO Staff

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Current as of 5/08

Dr. Greg Kovacs
Director

Dr. Dean R. Collins
Deputy Director

Mr. Robert Glaze
ADPM

Ms. Barbara Pica
Financial Management

Mr. Steve Larsen
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Dr. Stu Horn

Dr. Thomas Kenny

Dr. Amit Lal

Dr. Joe Mangano

Dr. Stephen A. Pappert

Dr. Dennis Polla

Dr. Sanjay Raman

Dr. Mark Rosker

Dr. Jagdeep Shah

Dr. Devanand K. Shenoy

Dr. Henryk Temkin

A little bit about me…

Circuit, Heal Thyself!

- **DARPA/MTO Program Manager as of Sep. 2007**
- **IPA from Virginia Polytechnic Institute & State University (Virginia Tech)**
  - Joined faculty in 1998, currently Associate Professor of ECE
- **Education**
  - BEE, Georgia Tech, 1987
  - MSEE, Univ. of Michigan, 1993
  - Ph.D. EE, Univ. of Michigan, 1998
- **US Navy Nuclear-trained submarine officer from 1987-1992**
- **Key interests**
  - RF/microwave/mm-wave & analog/mixed-signal ICs
  - 3D ICs and packaging technology
  - RF MEMS/NEMS
  - Integrated & Active antennas
  - Communications and Sensor microsystems

Dr. Sanjay Raman

TFAST

DARPA/MTO FLARE

Stay Tuned…

MTO Mixed-Signal Electronics/MEMS Programs for RF Applications

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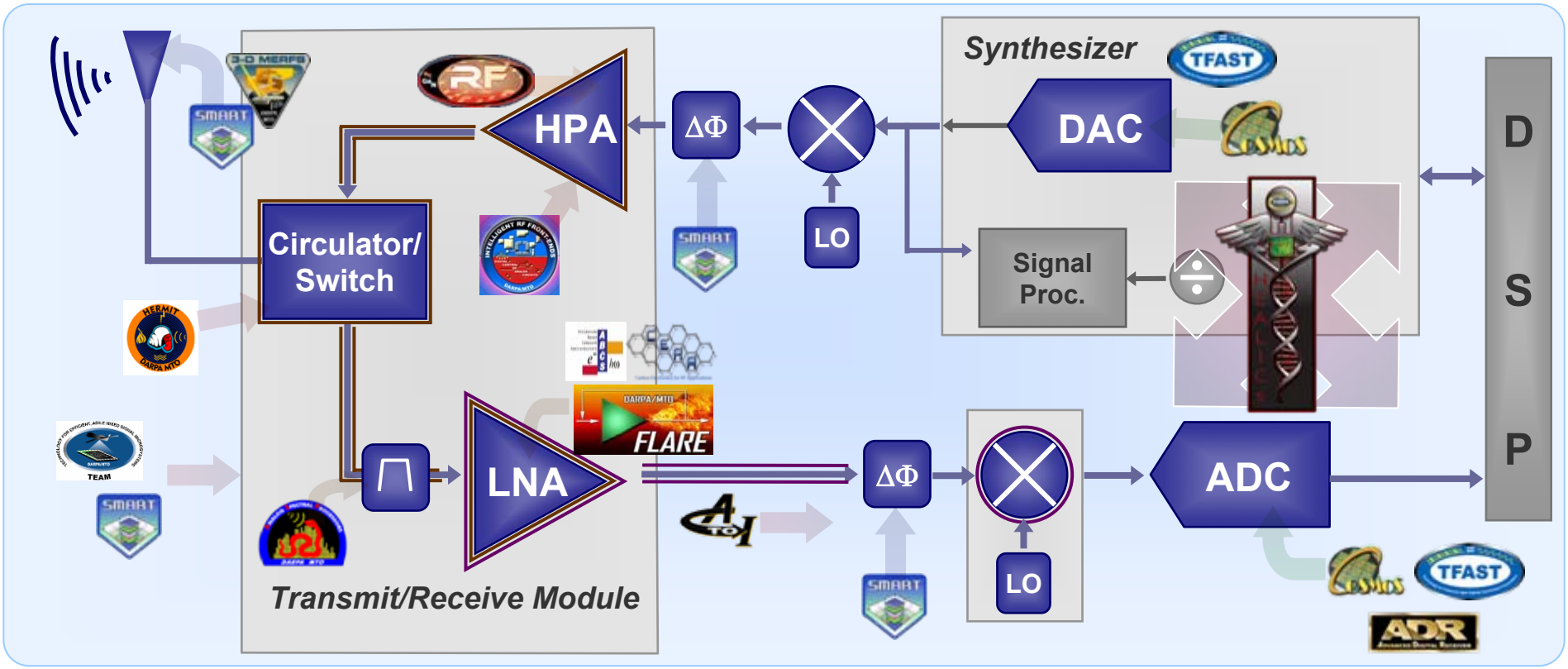
MTO's Current Programs ←→ Tomorrow's RF System Solutions



Advanced RF & Mixed-Signal Electronics + Self-Awareness/Intelligence/Adaptation

Enables → ***Network Centric Warfare*** ☑

Question Process

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- Please write your questions down on 3” x 5” cards
- Questions will be collected during the Contracting Presentation
- We will attempt to answer as many questions at this workshop as time will allow
- Answers to all questions will be posted subsequent to this meeting on the BAA 08-40 page: www.darpa.mil/mto/solicitations/baa08-40/index.html

  → FAQ link

The HEALICs Program

The Challenge

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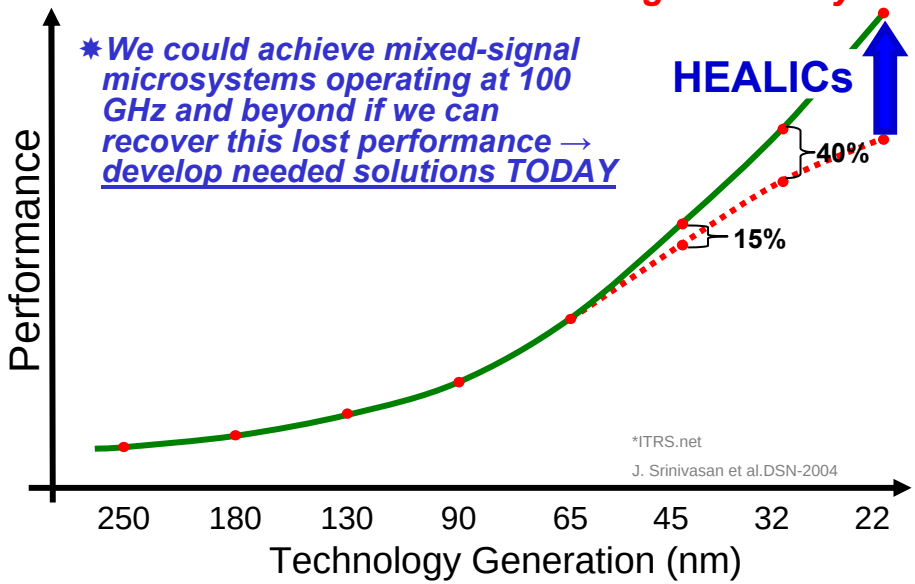
Performance Lost Due to Scaling Variability



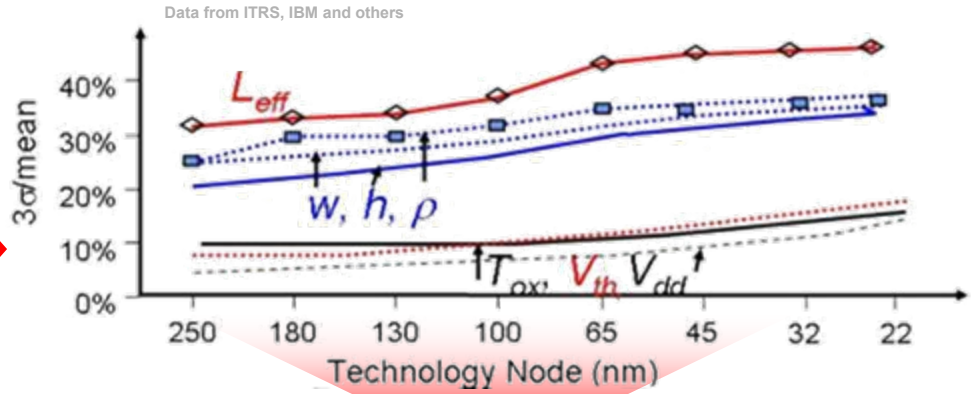
HEALICs

Achieve near 100% performance yield of DoD mixed-signal ICs in the presence of extreme technology variations

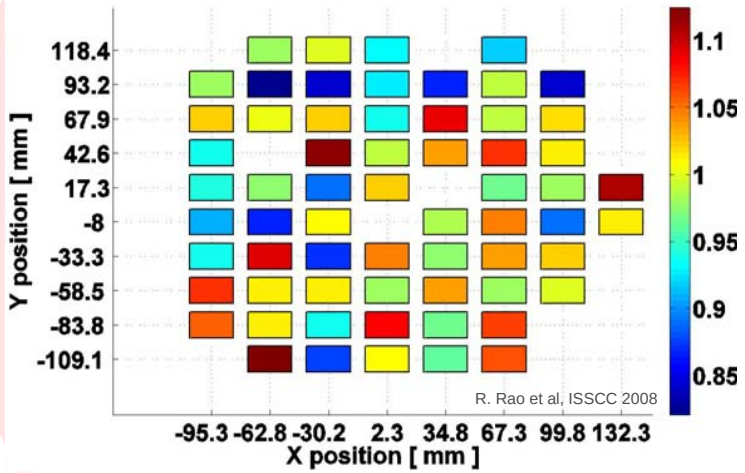
- **Develop novel circuit designs & control algorithms while minimizing added die area/power overhead**
- **Exploit large numbers of available digital devices for on-chip, self-healing management**
- **Minimize design cycles/times for mission critical DoD electronic systems**
- **Provide robustness in the presence of harsh environmental variations and long-term ageing**

The Problem

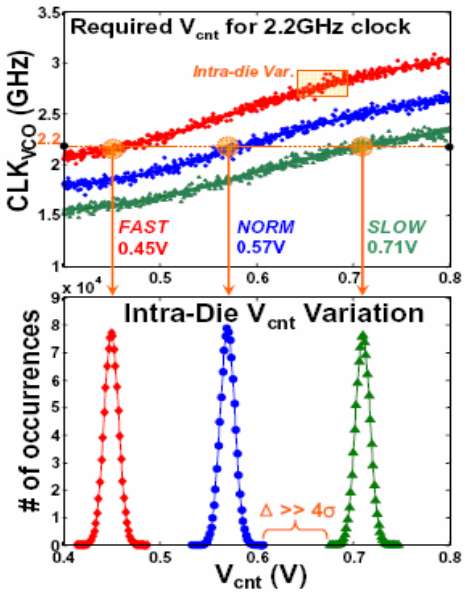
- **Extreme CMOS device variability in sub-50nm regime**
  - Due to dopant fluctuations, sub-λ lithograph, heat flux/temperature variation, etc.
- **Other technologies may experience severe variations at even less aggressive nodes**
- **DoD ICs susceptible to harsh environments, which further increases variability**
  - temperature, EMI/EMP, radiation effects, etc.
- **Less work to date on combating these effects in RF/Mixed-Signal ICs**
  - More focus on error correction/fault-tolerant design in microprocessors and memories



Parameter variations across a 45 nm tech. wafer



Example:
Process variations in 130nm CMOS technology cause the center frequency of an RF VCO to change significantly → required control voltage to tune to target frequency shifted by >> 4σ



Digital Resiliency Techniques

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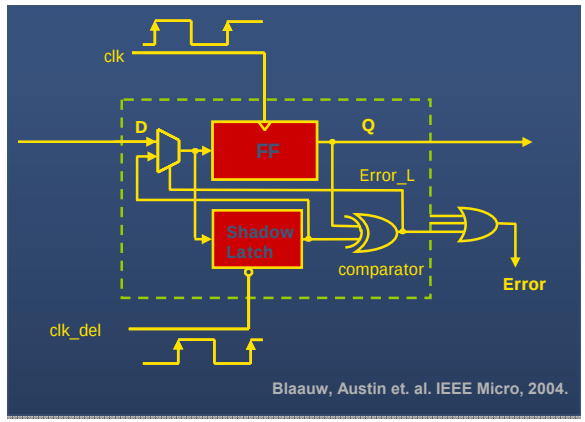
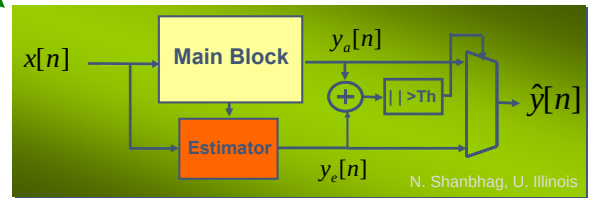
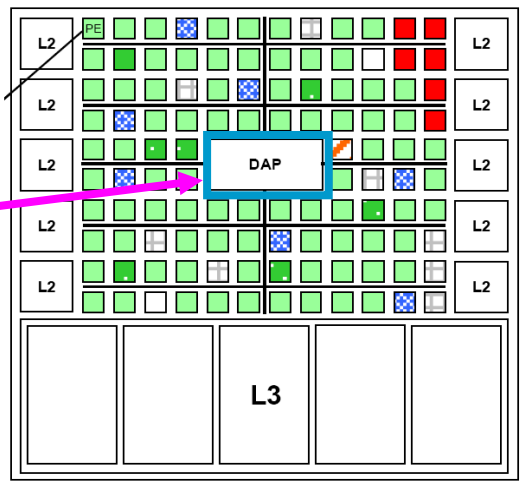
- **System level focus**
  - Using a combination of hardware and software solutions
- **Chip level approaches with embedded logic**
  - Redundant logic with a voting mechanism for different failure types
    - *Majority, Plurality or Threshold voting implementations*
  - Error checkers and correction logic
    - *Heavily used today for memories*
- **Multicore approach being taken by industry**
- **Ongoing resiliency work in FCRP/GSRC**
  - Focused on microprocessors
  - Redundant multi-core architectures for adaptability
  - Error-resilient system level techniques

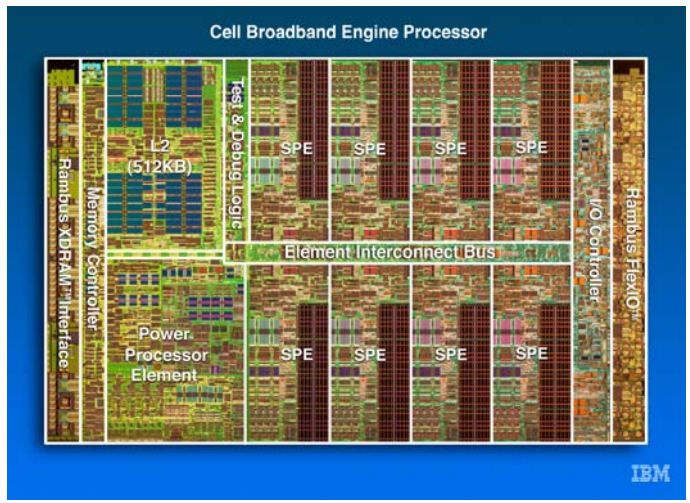




"Protected" Diagnostic Adaptivity Processor



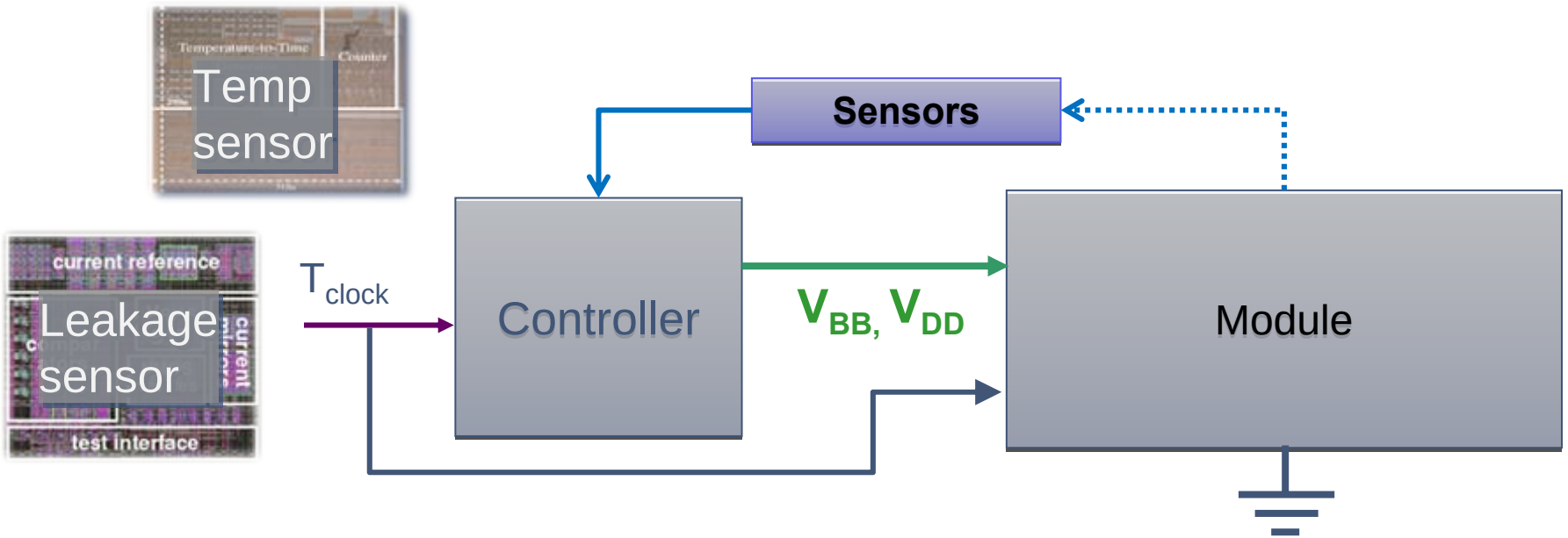
Blaauw, et. al. IEEE D&T, 2006.



“Always-Optimal” Systems

System modules are adaptively biased to adjust to operating, manufacturing and environmental conditions

- Parameters to be measured: temperature, delay, leakage
- Parameters to be controlled: V_{DD}, V_{TH} (or V_{BB}), or even functionality



- Minimum energy under technology and manufacturing limits
- Inherently improves the robustness of design timing
- Minimum design overhead required over the traditional design methodology

Mixed-Signal Circuit Techniques

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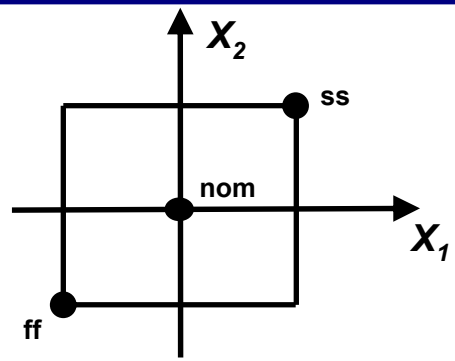
Status Quo:

- **Global and local device variations and temperature, bias, etc. variations must be handled**
- **Designers must validate all parameters within scope of anticipated process variations (corner analysis)**
  - ***Process variation characterization critical***
  - ***Extensive design, layout iteration and verification time needed***
- **Application-specific circuit design techniques used to compensate for variations, digital calibration/look-up tables to set parameters**

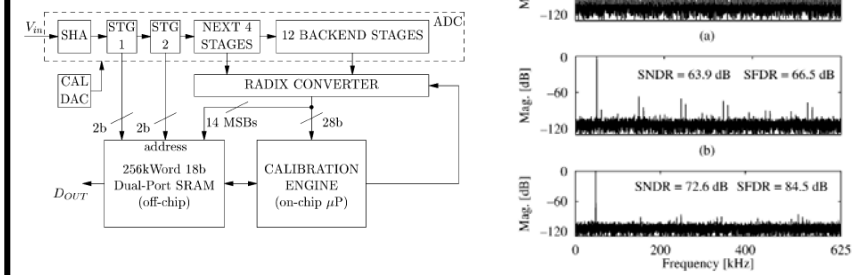


Worst Case Corner Analysis

Shannon Kurtas (Drexel) Statistical Static Timing Analysis 2007

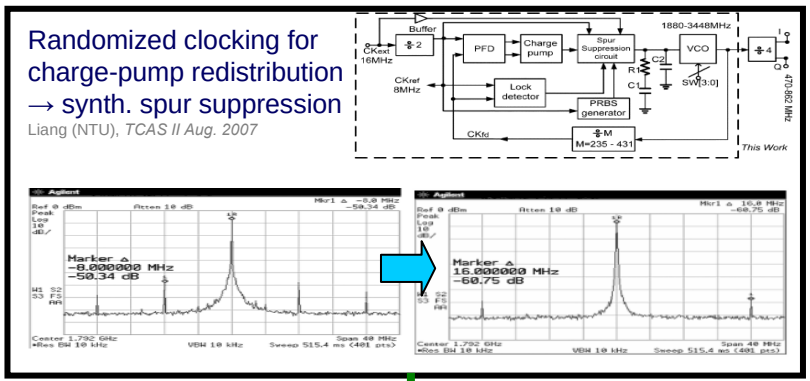
Digital Calibration → Improved ADC SFDR

Grace, Hurst, Lewis, *JSSC May 2005*

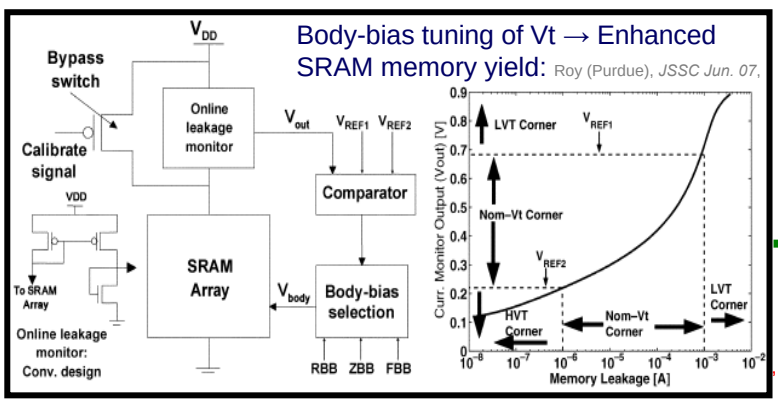


Randomized clocking for charge-pump redistribution → synth. spur suppression

Liang (NTU), *TCAS II Aug. 2007*



Body-bias tuning of Vt → Enhanced SRAM memory yield: Roy (Purdue), *JSSC Jun. 07,*



Need a unified approach to address process/environmental variability in mixed signal circuits

Vision

Near 100% Performance Yield of mixed-signal ICs

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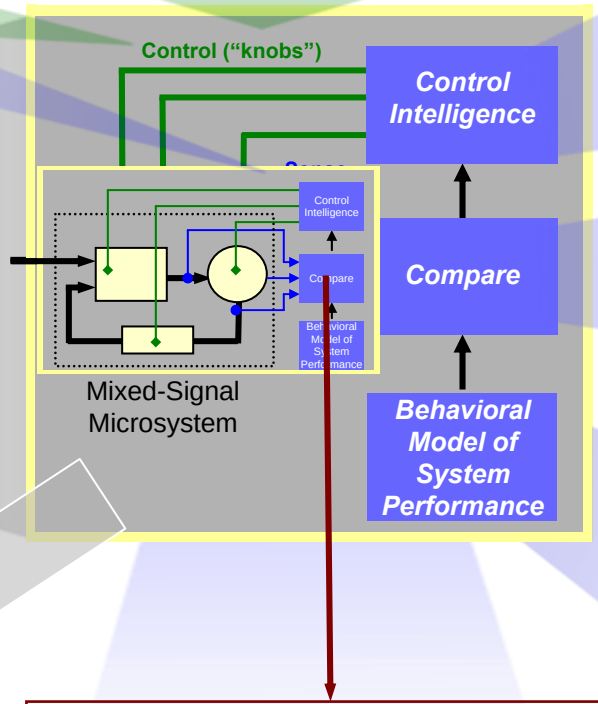
Self-healing mixed-signal ICs/SoCs

Identification and design of in-situ "knobs" and "meters" for dynamic performance correction

Switched device size, body bias, current, Gm, clock speed, delay, divider ratio, switched capacitors/varactors…



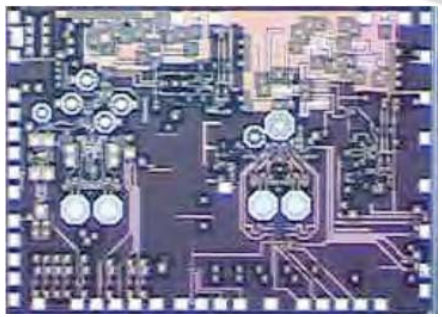
Development of robust/stable control algorithms & hardware implementations, must also be resistant to variability

Program integration, multi-disciplinary teams:

- Mixed-signal IC/SoC design
- Algorithms and control
- Advanced nano-scale technology/trusted foundry support
- Device modeling/CAD

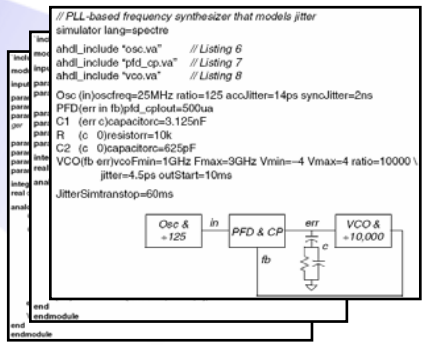
Comparison of behavioral models to local measurements & global performance to generate control inputs on-chip

Process variation



Environment **Ageing**

Externally perceived performance near-identical to ideal performance under extreme variability



Minimize power and die area overhead associated with on-chip integration of self-healing circuitry → 5% of baseline circuit

Integrated behavioral models → "mental image" of desired/"ideal" circuit performance.

Understand mapping between models and local/global parameters

HEALICs: Program Plan

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Proposal: Provide a complex baseline SoC design with identified mixed-signal core for Phase I demo, with demonstrated/predicted poor performance yield with respect to the proposer-specified target performance metrics

Phase I: Develop self-healing mixed-signal core for the proposed SoC

Phase II: Integrate self-healing mixed-signal core from Phase I into final large SoC

Phase I

Demonstrate Self-Healing Mixed-Signal Core

Development

- Local self-healing control for individual sub-blocks (anticipated transistor counts in the 100-1k range) within larger mixed-signal core
- Integration of sub-blocks into larger mixed-signal core (anticipated transistor counts in the 100-1k range) and development of global self-healing algorithms

Demonstration

- Increase in performance yield of mixed-signal core from baseline value to at least 75% upon activation of self-healing
- Maximum of 10% power/die area overhead relative to baseline design

Phase II

Demonstrate Self-Healing Mixed-Signal Microsystem/SoC

Development

- Integration of previously demonstrated Phase I mixed-signal core into full microsystem/SoC (anticipated transistor counts in the 100k-1M range)
- Global self-healing control at the microsystem/SoC level

Demonstration

- Increase in performance yield of full SoC from baseline value to at least 95% upon activation of self-healing
- Maximum of 5% power/die area overhead relative to baseline design

Program Metrics

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Metric	Phase I: Mixed-Signal Core	Phase II: Mixed-Signal SoC
Performance Metrics that Define Performance Yield	Performer Defined and Circuit Specific	Performer Defined and Circuit Specific
Performance Yield	> 75% of die per wafer meet all performance specs	> 95% of die per wafer meet all performance specs
Power Consumption Overhead	< 10% over baseline circuit	< 5% over baseline circuit

Performance yield without self-healing = D_0/N_0 where,
D_0 = # of baseline die meeting *all* performance requirements, and
N_0 = # of testable baseline die (without self-healing) per wafer

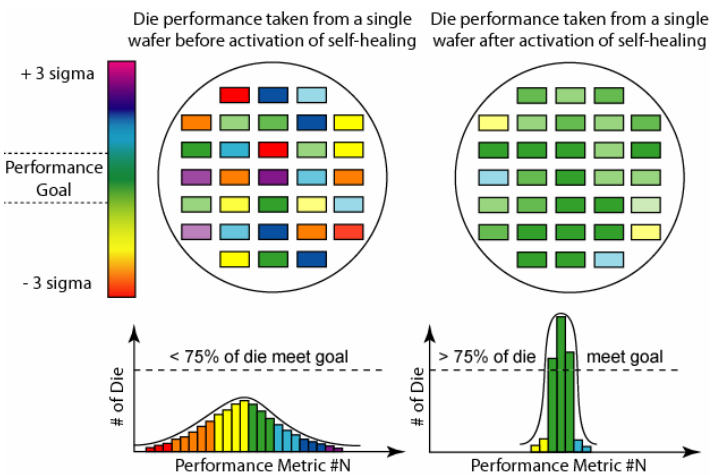
Performance yield *with* self-healing = $D_{HEALICs}/N_0$ where,
$D_{HEALICs}$ = # of die meeting *all* performance requirements with self-healing activated.
Performance yield with self healing is referenced to the number of baseline die N_0 in order to account for the potentially reduced number of self-healing die per wafer due to the additional circuitry.

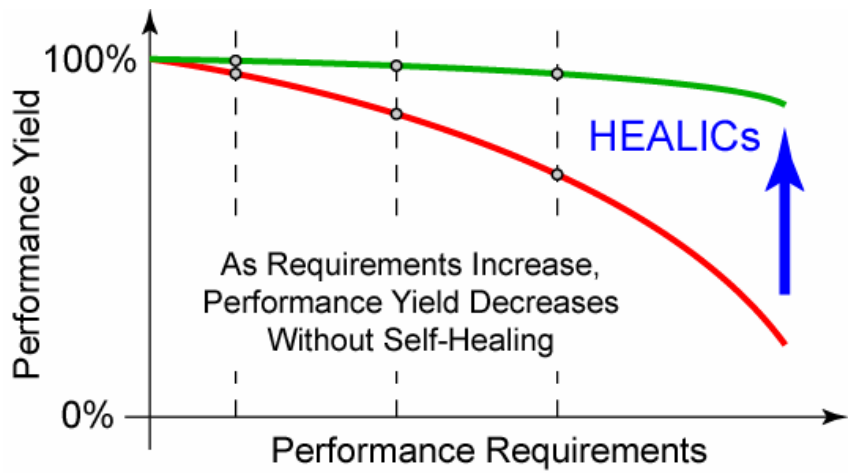
A statistically significant number of die should be tested for the calculation of the performance yield.

What constitutes a Baseline design?

1. Fabricated design with poor (near zero) performance yield
2. Fabricated design has acceptable performance yield with respect to "backed-off" performance specifications → but increasing performance requirements results in poor (near zero) performance yield
3. Simulated design predicted to have poor (near zero) performance yield that was not fabricated for this reason

** Baseline design power consumption (all modes) and die area defined for subsequent comparison to self-healing designs*





Example Mixed-Signal Cores/SoCs

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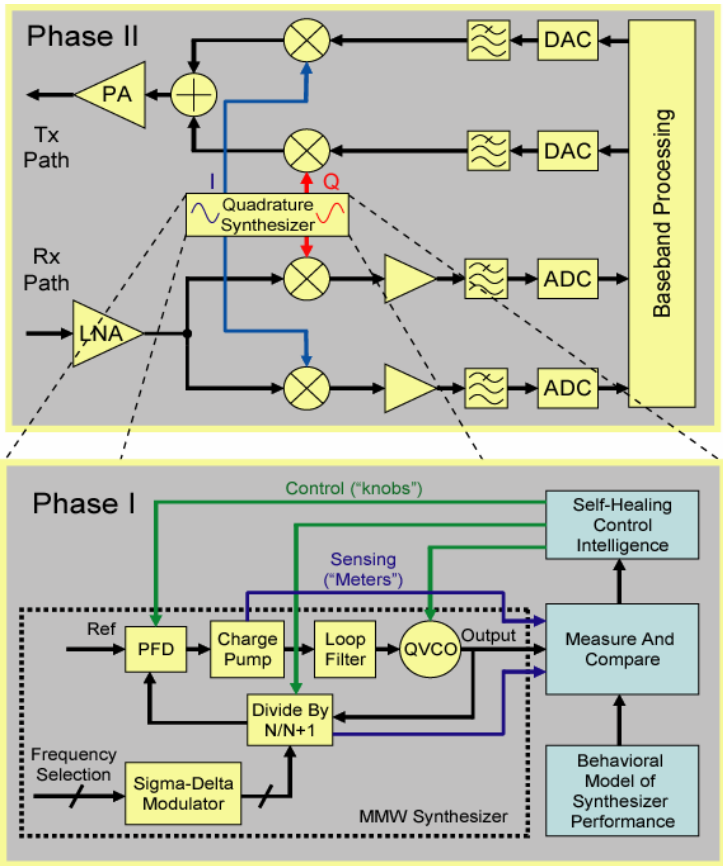
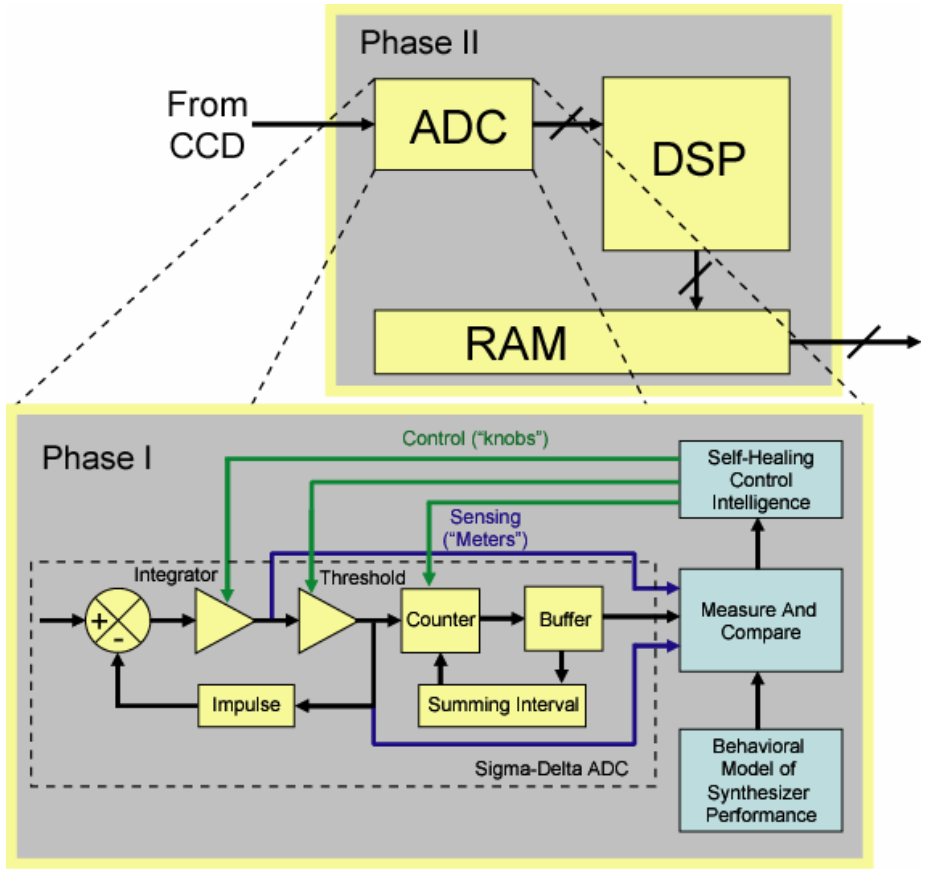
Example 1 SoC: mmW Transceiver
Mixed-Signal Core: Frac-N Synth.



Example 2 SoC: Video Compression DSP
Mixed-Signal Core: Σ-Δ ADC



- **These are examples only, these should NOT be construed as the only types of circuits of interest**
- **Numbers of transistors for each phase mentioned in BAA are *anticipated* ranges, not metric values**

Proposal Evaluation Criteria

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- **It is critical that the proposal be responsive to all BAA requirements, including page limits and formatting requirements.**
- **Read the BAA section on Evaluation Criteria, section V.A, starting on pg. 25, very carefully. The evaluation criteria in *descending* order of importance are given below…**

a) ***Ability to meet program G/NG Metrics –*** Note that we have both government-defined and proposer-defined metrics. The proposal should establish clear and well-defined metrics appropriate to the proposed mixed-signal IC/SoC, and these will be used in the evaluation of performance yield.

b) ***Overall Scientific and Technical Merit –*** "The proposal identifies major technical risks and planned mitigation efforts are clearly defined and feasible."

c) ***Potential Contribution and Relevance to the DARPA Mission –***

d) ***Realism of Proposed Schedule –*** you should propose a schedule that is appropriate to the proposed scope of work.

e) ***Proposer's Capabilities and/or Related Experience –*** Note that we cannot give you specific guidance on forming your teams, the composition of the team should be appropriate to the proposed SoW. Note that completed/ongoing efforts by the proposer in this area must fully described including identification of other Government sponsors.

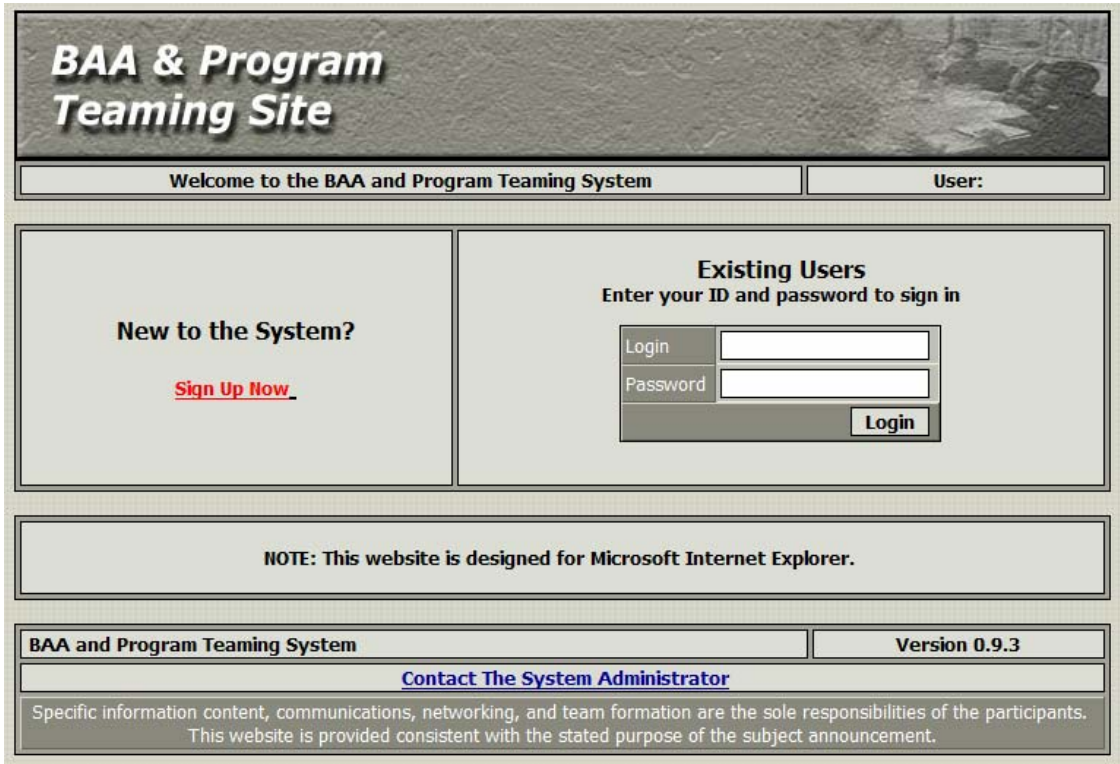
f) ***Plans and Capability to Accomplish Technology Transition –*** addressing this criteria may help in making teaming decisions

g) ***Cost Realism –*** the proposed budget should be appropriate to the proposed SoW.

Teaming

- **Collaborative efforts/Teaming is highly encouraged**
- **A subsequent presentation will discuss the teaming website.**

http://www.davincinetbook.com/teams/



PENTA-CHART
(remove from slide)

Performer Name
Topic/project/effort description

Cost by Phase
Schedule by Phase

STATUS QUO

What is the state of the art and what are its limitations?

(DELETE THIS BOX OF TEXT AND INSERT DIAGRAM(S)

Primary answer here. Add more text as necessary.

- *First bullet point*
- *Additional as necessary*

NEW INSIGHTS

What are the key new insights?

(REPLACETHIS BOX AND INSERT DIAGRAM(S))

First key insight. Add more text as necessary.

Second key insight. Add more text as necessary.

- Add other points as necessary

PROPOSED GOAL(S):

Placeholder explanatory text. Replace with text and diagrams as necessary.

HOW IT WORKS:

Placeholder explanatory text paragraph. Replace with text and diagrams as necessary.

ASSUMPTIONS AND LIMITATIONS:

- Limitation or assumption
- Another limitation or assumption

QUANTITATIVE IMPACT

CHARACTERIZE THE QUANTITATIVE IMPACT

(DELETE THIS BOX OF TEXT AND INSERT TABLE, GRAPH, OR OTHER SUITABLE VISUALIZATION)

First item planned. Add more text as necessary.

Second item planned. Add more text as necessary.

- Add other points as necessary

END-OF-PHASE GOAL

What are the end-of-phase deliverables?

(REPLACE WITH DIAGRAM/TEXT/THRESHOLD CRITERIA)

Primary answer here. Add more text as necessary.

- *First key point*
- *Additional as necessary*

A sentence why it is important/useful

Important Dates

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- **July 3rd, 2008 – Abstracts due in TFIMS, 4:00 PM EDT**
- **Approximately July 30th, 2008 – Encourage/ discourage feedback provided on Abstracts**
- **August 12th – Last date to ask questions for answers to be posted on-line**
- **Sept. 3rd, 2008 – Full proposals due, 4:00 PM EDT**